Electronic Version
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Claims

[c1] 1. A high density semiconductor package, comprising:
a substrate, having a surface;
a first package module, being disposed on the surface of the substrate; and
four second package modules, being disposed on the surface of the substrate surrounding the first package module.

[c2] 2. The high density semiconductor package as claimed in claim 1, wherein a gap width between the second package modules and the first package module is larger than 2 mm.

[c3] 3. The high density semiconductor package as claimed in claim 1, wherein the first package module comprises:
a chip;
a plurality of bumps located between the chip and the substrate; and
an underfill located between the chip and the substrate and enveloping the bumps.

[c4] 4. The high density semiconductor package as claimed in claim 1, wherein each of the second package modules

comprises:

a chip;

a plurality of bumps located between the chip and the substrate; and

an underfill located between the chip and the substrate and enveloping the bumps.

[c5] 5. A high density semiconductor package, comprising:

a substrate having a surface;

a first package module, being disposed on the surface of the substrate; and

four second package modules, being disposed on the surface of the substrate surrounding the first package module, wherein a gap width between the first package module and the second package modules is large enough to fill an underfill material therein.

[c6] 6. The high density semiconductor package as claimed in claim 5, wherein the gap width between the second package modules and the first package module is larger than 2 mm.

[c7] 7. The high density semiconductor package as claimed in claim 5, wherein the first package module comprises:

a chip;

a plurality of bumps located between the chip and the substrate; and

an underfill located between the chip and the substrate and enveloping the bumps.

[c8] 8. The high density semiconductor package as claimed in claim 5, wherein each of the second package modules comprises:
a chip;
a plurality of bumps located between the chip and the substrate; and
an underfill located between the chip and the substrate and enveloping the bumps.

[c9] 9. The high density semiconductor package as claimed in claim 5, wherein the first package module is arranged substantially orthogonal to the second package modules.

[c10] 10. The high density semiconductor package as claimed in claim 5, wherein the first package module is arranged substantially non-orthogonal to the second package modules.

[c11] 11. A high density semiconductor package, comprising:
a substrate, having a surface;
a first package module, being disposed on the surface of the substrate; and
a plurality of second package modules, being disposed on the surface of the substrate surrounding the first

package module, wherein a corner of each of the second package modules face a side of the first package module.

[c12] 12. The high density semiconductor package as claimed in claim 11, wherein a gap width between the second package module and the first package module is larger than 2 mm.

[c13] 13. The high density semiconductor package structure as claimed in claim 11, wherein the first package module is arranged coplanar with the second package modules.

[c14] 14. The high density semiconductor package as claimed in claim 11, wherein the first package module comprises:
a chip;
a plurality of bumps located between the chip and the substrate; and
an underfill located between the chip and the substrate and enveloping the bumps.

[c15] 15. The high density semiconductor package as claimed in claim 11, wherein each of the second package modules comprises:
a chip;
a plurality of bumps located between the chip and the substrate; and

an underfill located between the chip and the substrate and enveloping the bumps.

[c16] 16. A high density semiconductor package at least comprising:
a substrate, having a surface;
a first package module, being disposed on the surface of the substrate; and
at least one package module, being adjacent to the first package module with a gap width between the first package module and the second package modules being large enough to fill an underfill material therein.

[c17] 17. The high density semiconductor package as claimed in claim 16, wherein the gap width between the second package module and the first package module is larger than 2 mm.

[c18] 18. The high density semiconductor package as claimed in claim 16, wherein the first package module is coplanar with the second package module.

[c19] 19. The high density semiconductor package as claimed in claim 16, wherein the second package module are disposed on the surface of the substrate.

[c20] 20. The high density semiconductor package as claimed in claim 16, wherein the first package module comprises:

a chip;

a plurality of bumps located between the chip and the substrate; and

an underfill located between the chip and the substrate and enveloping the bumps.

[c21] 21. The high density semiconductor package as claimed in claim 16, wherein the second package module comprises:

a chip; and

a plurality of bumps located between the chip and the substrate; and

an underfill located between the chip and the substrate and enveloping the bumps.

[c22] 22. The high density semiconductor package as claimed in claim 16, wherein the first package module is arranged substantially orthogonal to the second package module.

[c23] 23. The high density semiconductor package as claimed in claim 16, wherein the first package module is arranged substantially non-orthogonal to the second package module.